What is claimed is:

1. A semiconductor device comprising:

a semiconductor chip having a first main surface on which a plurality of electrode pads is provided, a second main surface which opposes said first main surface, and a plurality of side surfaces between said first main surface and said second main surface;

an extension portion which includes a first face and a second face opposing said first face, and which is formed in contact with said side surfaces of said semiconductor chip to thereby surround said semiconductor chip and such that said first face is at a substantially equal level to the level of said first main surface;

a base having a first surface and a second surface which opposes said first surface, said first surface contacting the second face of said extension portion and the second main surface of said semiconductor chip, which is capable of conducting heat generated by said semiconductor chip such that this heat is dispersed into the atmosphere from said second surface side;

an insulating film which is formed on said first face and said first main surface such that a part of each of said plurality of electrode pads is exposed;

a plurality of wiring patterns electrically connected to said electrode pads and extended from said electrode pads to the upper side of the first face of said extension portion, respectively;

a sealing portion which is formed on said wiring patterns and said insulating film such that a part of each of said wiring patterns is exposed; and

a plurality of external terminals provided over said wiring patterns in a region including the upper side of said extension portion.

2. A semiconductor device comprising:

a semiconductor chip comprising a first main surface on which a plurality of electrode pads is provided, a second main surface which opposes said first main surface, and a plurality of side surfaces between said first main surface and said second main surface;

an extension portion having a concave portion with inclined inside walls, which comprises a first face and a second face opposing said first face, and which is formed in contact with said side surfaces of said semiconductor chip to thereby surround said semiconductor chip and such that said first face is at a substantially equal level to the level of said first main surface;

a base comprising a first surface and a second surface which opposes said first surface, said first surface contacting and thus supporting the second face of said extension portion and the second main surface of said semiconductor chip, which is capable of conducting heat generated by said semiconductor chip such that this heat is dispersed into the atmosphere from said second surface side;

an insulating film which is formed on the surface

of said inside walls, the surface of said extension portion, and said first main surface such that a part of said electrode pads is exposed;

a plurality of wiring patterns electrically connected to each of said electrode pads and extended from said electrode pads to the upper side of the first face of said extension portion;

a sealing portion which is formed on said wiring patterns and said insulating film such that a part of said wiring patterns is exposed; and

a plurality of external terminals provided on said wiring patterns in a region including the upper side of said extension portion.

3. The semiconductor device according to claim 1, further comprising a plurality of electrode posts formed between said wiring patterns and said external terminals,

wherein said sealing portion is formed such that the top surface of said electrode posts is exposed.

4. The semiconductor chip according to claim 3, wherein said electrode posts are formed from a conductive material.

5. The semiconductor device according to claim 4, wherein a thin oxidation layer is formed on the surface of said electrode posts.

6. The semiconductor device according to claim 1, wherein a portion of said wiring patterns on a boundary and vicinity thereof between a region on the upper side of said semiconductor chip and a region of said extension portion is

formed wider or more thickly than other portions of said wiring patterns.

7. The semiconductor device according to claim 1, wherein said extension portion is formed from a material having greater molding shrinkage than the molding shrinkage of said sealing portion.

8. The semiconductor device according to claim 1, wherein said extension portion is formed from a liquid resin having a coefficient of linear expansion, within a lower temperature range than a glass transition temperature, of less than $1.5 \times 10^{-5}/°C$ and a modulus of elasticity within a range of 7.8 to 22 GPa.

9. The semiconductor device according to claim 1, wherein said second face of said base is formed as a three-dimensional construction in which the surface area of said second face is increased.

10. The semiconductor device according to claim 1, wherein said base is formed from a material having a thermal conductivity of at least 150W/m · K.

11. The semiconductor device according to claim 1, wherein said base is formed from either a metallic material selected from a group including copper (Cu), aluminum (Al), and a copper/tungsten alloy (CuW), or a ceramic material selected from a group including silicon carbide (SiC) and aluminum nitride (AlN).